REMARKS

In response to the above-identified Final Office Action, Applicant amends the application and seeks reconsideration thereof. In this response, Applicant amends claims 8 and 15. Applicant does not cancel or add any new claims. Accordingly, claims 8-10, 13-17 and 20-21 are pending.

I. Claims Rejected Under 35 U.S.C. §103(a)

The Patent Office rejects claims 8-10, 13-17, 20 and 21 under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 4,015,281 issued to Nagata et al. ("Nagata") in view of U.S. Patent No. 5,990,516 issued to Momose et al. ("Momose") and U.S. Patent No. 5,621,681 issued to Moon ("Moon"). Applicant amends claims 8 and 15.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. See MPEP § 2143. Applicant respectfully submits the combination of Nagata, Momose and Moon fails to teach or suggest each of the elements in the claims, as amended.

Regarding the rejection of claim 8, among other elements, claim 8 defines a transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate comprising a first and second dielectric material being scalable for a set of feature size technologies, the set of feature size technologies defined by a gate length in the range of 25-70 nm wherein the first material thickness and second material thickness are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$ and wherein the transistor device is isolated from other devices by shallow trench isolation structures. In making the rejection, the Patent Office characterizes Nagata as showing "a transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate." See Paper No. 20040405, page 2 (citing col. 3, line 45 to col. 4, line 67). In addition, the Patent Office alleges Nagata teaches that the dielectric "comprises a first dielectric having a first dielectric constant and a second dielectric having a second dielectric constant different from the first

dielectric constant." Id. (citing col. 4, lines 34-49). Moreover, the Patent Office states, "the first and second dielectrics are scalable for a set of feature sized technologies, wherein the first and second dielectric thickness are determined by the formula as recited in claims 8 and 15 (see the expanded formula in col. 4, lines 39-49)." Paper No. 20040405, page 2. The Examiner does not cite Nagata for teaching that the transistor device is isolated from other devices by shallow trench isolation structures. In addition, Applicant in reviewing Nagata in its entirety cannot find any sections that teach or suggest a transistor device isolated from other devices by shallow trench structures.

Moreover, Applicant respectfully submits that Nagata cannot be modified to include shallow trench structures because doing so would render the device in Nagata unsatisfactory for its intended purpose. See MPEP §2143.01. Since it is desirable for MIS-FETs to be placed electrically close to each other on a substrate to conserve real estate, a short-circuit may be caused by a parasitic MIS-FET. See Nagata col. 1, lines 17-27. To isolate the transistors in Nagata from each other so that the parasitic MIS-FET does not occur, a plurality of isolating film layers are oriented on the surface of the substrate between the transistors to induce holes in the surface portion so that parasitic a MIS-FET's gate electrode, which is the metal interconnection deposited on the insulating film, will be unable to operate. See Nagata col. 1, lines 27-33. Therefore, Applicant respectfully submits that using a trench in Nagata would not sufficiently cure the parasitic problems in Nagata since a parasitic MIS-FET's gate electrode would still be able to operate. In other words, the parasitic MIS-FET's gate electrode would still be operable and would likely could a short-circuit, the prevention of which is the desired result of Nagata. Thus, Nagata fails to teach or suggest each of the elements of claim 8. The Examiner relies on Momose to cure the defects of Nagata.

The Patent Office characterizes Momose as showing "a semiconductor device having double layer gate dielectric in which the feature size technology has a gate length of 150 nm (or 0.15 μm) to form a high performance semiconductor having low power consumption." Paper No.20040405, page 3 (citing Momose, col. 16, lines 28-48 and col. 16, line 66 – col. 17, line 32). The Patent Office further characterizes Momose as showing that the gate length can be decreased

even more to improve the current drive capability and in one embodiment had a length of 40 nm. See Id., page 3 (citing Momose, col. 15, lines 13-31). In addition, the Patent Office alleges Momose shows one embodiment having a gate dielectric which is less than 1/3 the gate length. See Paper No. 20040405, page 3 (citing Momose col. 2, lines 52-58). The Patent Office does not cite Moon as teaching or suggesting a transistor device isolated from other devices shallow trench structures as defined in claim 8. Moreover, in reviewing Momose in its entirety, Applicant is unable to find any sections that teach or suggest such elements. Therefore, Momose fails to cure the defects of Nagata.

The Patent Office relies on Moon to cure the defects of Nagata and Momose. However, similar to the discussion above regarding Momose, the Patent Office does not cite Moon as teaching or suggesting a transistor device a transistor device isolated from other devices by shallow trench structures as defined in claim 8. In addition, in reviewing Moon in its entirety, Applicant is unable to discern any sections that teach or suggest at least these elements. Therefore, Moon fails to cure the defects of Nagata and Momose.

The failure of the combination of Nagata, Momose and Moon to teach or suggest each of the elements of claim 8 is fatal to the obviousness rejection. Therefore, claim 8 is not obvious over Nagata in view of Momose and Moon. Accordingly, Applicant respectfully requests withdrawal of the rejection of independent claim 8.

Claims 9-10 and 13-14 each depend from claim 8 and contain each of the elements thereof. Therefore, claims 9-10 and 13-14 are not obvious over Nagata in view of Momose and Moon at least for the same reasons as claim 8. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 9-10 and 13-14.

Regarding the rejection of claim 15, among other elements, claim 15 defines a semiconductor substrate having a transistor device formed thereon, the transistor device isolated from other devices by shallow trench structures and having a gate dielectric disposed directly between a surface of the substrate and a gate electrode comprising a first dielectric material selected from the group consisting of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2 and having a first dielectric

constant and a second dielectric material having a second dielectric constant different from the first dielectric constant, the first and second dielectric materials being scalable for each of a plurality of feature size technologies, having a gate length in the range of 25-70 nm, and wherein the first material thickness and the second material thickness are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$ similar to claim 8. Therefore, Applicant respectfully submits the discussion above regarding the combination of Nagata, Momose and Moon failing to teach or suggest at least a transistor device isolated from other devices by shallow trench structures is equally applicable to similar elements defined in claim 15. Therefore, claim 15 is not obvious over Nagata in view of Momose and Moon. Accordingly, Applicant respectfully requests withdrawal of the rejection of claim 15.

Claims 16-17 and 20-21 depend from claim 15 and contain each of the elements thereof. Therefore, claims 16-17 and 20-21 are not obvious over Nagata in view of Momose and Moon at least for the same reasons as claim 15. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 16-17 and 20-21.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Patent Office believes that a telephone conference would be useful in moving the application forward to allowance, the Patent Office is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 6/7/04

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 6/7/04.

Nadya Gordon 6/7/04

Nadya Gordon *Date*